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(54) SOLID-STATE IMAGE PICKUP DEVICE FOR MOVEMENT DETECTION

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a device which does not need image comparison processing and has an electronic shutter by reading an electric signal of the current frame to a vertical read line, comparing the electric signal of a preceding frame that is read in time sharing through the vertical read line with the electric signal of the current frame, horizontally transferring an output from a comparator circuit, discharging unneeded charge that is generated by a light receiving part and limiting the storage time of signal charge.

SOLUTION: A movement detection signal is generated when a moving object detection circuit 21b takes finite difference of an electric signal for two frames that are subjected to time division output to a vertical read line 12. Then, to perform movement detection, there is no need to provide peripheral circuits such as an AD conversion circuit, image

memory and an image processing circuit outside this solid-state image pickup device. As a result, it is possible to configure the entire devices such as a monitoring device and an image compressing device which need movement detection in small sizes and also at low costs. By generating a movement detection signal not through the AD conversion circuit, it is possible to perform movement with a dynamic range prevented from being limited.

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CLAIMS

[Claim(s)]

[Claim 1] Two or more light sensing portions which are arranged in the shape of a matrix and generate a signal charge according to incident light, The amplifier which is prepared for said every light sensing portion, has the regulatory region which accumulates a charge, and outputs the electrical signal corresponding to the stored charge of this regulatory region, The reset circuit which resets the regulatory region of said amplifier, and the charge transfer circuit which transmits the signal charge generated by said light sensing portion to the regulatory region of said amplifier, The perpendicular read-out line formed for every vertical file of said light sensing portion, and the readout circuitry which reads the electrical signal which is established for said every amplifier and outputted from said amplifier to said perpendicular read-out line, In the condition [intercepting said

charge transfer circuit and having made the signal charge of a front frame freely hold to said regulatory region] The front frame perpendicular transfer means which drives said readout circuitry of a specific line alternatively, and reads the electrical signal of a front frame to said perpendicular read-out line, Drive said charge transfer circuit of said specific line, and the signal charge of the present frame is made to hold to said regulatory region. In this condition The present frame perpendicular transfer means which drives said readout circuitry of said specific line, and reads the electrical signal of the present frame to said perpendicular read-out line, The comparator circuit which compares the electrical signal of a front frame and the electrical signal of the present frame which are established for said every perpendicular read-out line, and are read to time sharing through said perpendicular read-out line, The level transfer circuit which carries out the level transfer of each output from said comparator circuit, and the unnecessary charge discharge circuit which discharges the unnecessary charge which is prepared for said every light sensing portion, and is generated by said light sensing portion, The solid state camera for motion detection characterized by having the electronic shutter circuit which discharges the unnecessary charge generated by said light sensing portion through said

unnecessary charge discharge circuit during the cutoff period of said charge transfer circuit, and restricts the storage time of said signal charge in said light sensing portion.

[Claim 2] The solid state camera for motion detection which incorporates alternatively either the electrical signal of the front frame read to time sharing through said perpendicular read-out line, or the electrical signal of the present frame, and is characterized by having the picture signal output circuit which carries out a level transfer in the solid state camera for motion detection according to claim 1.

[Claim 3] In the solid state camera for motion detection according to claim 2, after the regulatory region of said amplifier has been initialized by the fixed electrical potential difference by the drive of said reset circuit The dark signal perpendicular transfer means which reads the electrical signal (dark signal) which drives said readout circuitry of a specific line alternatively, and is outputted from said amplifier to said perpendicular read-out line, It has the sample circuit which carries out the sample of said dark signal read to time sharing through said perpendicular read-out line. Said picture signal output circuit The solid state camera for motion detection characterized by outputting the signal which

subtracted the part of said dark signal by which the sample was carried out to said sample circuit from either the "electrical signal of a front frame", or the "electrical signal of the present frame."

[Claim 4] Said comparator circuit is a solid state camera for motion detection characterized by being the circuit where the electrical signal of the present frame and the electrical signal of a front frame judge whether it is in tolerance in the solid state camera for motion detection given in any 1 term of claim 1 thru/or claim 3, and is in agreement, and output a binary-ized signal according to the truth of a judgment result.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the solid state camera for motion detection which detects by moving based on an inter-frame difference. Especially this invention relates to the solid state camera for motion detection equipped with electronic shutter ability.

[0002]

[Description of the Prior Art] Conventionally, image data is picturized one by one through a solid state camera, and the image processing system for motion detection which performs dynamic body detection from the inter-frame difference of these image data is known. Drawing 9 is drawing showing this kind of image processing system 100 for motion detection. In drawing 9 , the image processing

system 100 for motion detection consists of the solid state camera 101, an AD translation circuit 102 which changes the picture signal (analog signal) from a solid state camera 101 into a digital signal, the image memory (the 1st image memory) 103 and image memory (the 2nd image memory) 104 where the digital signal from the AD translation circuit 102 is saved, and an image-processing circuit 105 which compares mutually the digital image data saved in this image memory 103,104, and detects a motion.

[0003] In such an image processing system 100 for motion detection of a configuration, after the picture signal (analog signal) of the 1st frame acquired with the solid state camera 101 is first changed into a digital signal in the AD translation circuit 102, it is saved in the 1st image memory 103. Next, in the 2nd frame which follows the 1st frame (the last frame), after the picture signal (analog signal) acquired by the solid state camera 101 is changed into a digital signal in the AD translation circuit 102, it is saved in the 2nd image memory 104.

[0004] In the image-processing circuit 105, a pixel which is different beyond a predetermined value as compared with a pixel unit in the digital signal saved in the 1st image memory 103 and the digital signal saved in the 2nd image memory 104 is detected. Such an inter-frame comparison enables it to perform dynamic

body detection in a photographic subject.

[0005]

[Problem(s) to be Solved by the Invention] However, in the above-mentioned conventional image processing system 100 for motion detection, there was fault that the circumference circuit of a solid state camera 101 was complicated, and became the image processing system 100 whole for motion detection is enlarged, and expensive. Moreover, the picture signal outputted from a solid state camera 101 is an analog signal, and is supplied to the AD translation circuit 102 with the analog signal. Therefore, the transmission line of an analog signal will be taken about and the fault of being easy to be influenced of ambient noise was also produced.

[0006] Furthermore, in the above-mentioned conventional image processing system 100 for motion detection, the dynamic range of a picture signal (analog signal) is restricted in the AD translation circuit 102. Usually, since the input dynamic range of the AD translation circuit 102 was narrower than the dynamic range of a solid state camera 101, the large dynamic range of a solid state camera 101 also had the fault that it could not use effectively, in process of detection processing of a dynamic body.

[0007] Moreover, in the external image-processing circuit 105, when the comparison with the electrical signal of a front frame and the electrical signal of the present frame was performed, a possibility that slight phase gap might arise was in the pixel location which should be compared for the synchronous gap at the time of the conversion in the AD translation circuit 102 etc. Since an inter-frame difference was produced in an edge part etc. even if it is a quiescence object when such phase gap arises, the fault that the precision and dependability of dynamic body detection became remarkably low had been produced.

[0008] In order to avoid the above faults, preparing the memory for memorizing the picture signal in the last frame and the present frame for every pixel of a solid state camera 101, preparing the comparator circuit which compares the picture signal further memorized by this memory for every pixel, and generating the signal with which a dynamic body is expressed for every pixel is also considered. However, as such a cure, the structure of each pixel becomes complicated and the fault of causing decline in the numerical aperture of a solid state camera 101 and the fall of resolution arises.

[0009] Furthermore, as the above-mentioned cure, since only each pixel

lost-motion detecting signal was outputted, there was also fault of not being obtained by coincidence, about the picture signal which should be originally outputted in a solid state camera. Moreover, as the above-mentioned cure, since the structure of each pixel becomes complicated, it becomes difficult from on a semi-conductor tooth space to add electronic shutter ability for every pixel.

[0010] When an image flows by early motion of a photographic subject especially, it becomes impossible from an inter-frame difference to detect the location of a dynamic body etc. correctly. Therefore, it is desirable practically to have electronic shutter ability as equipment for motion detection, and it becomes important to meet such a request. So, it aims at the thing which made image comparison processing outside unnecessary in motion detection, and was equipped with electronic shutter ability and for which it moves and the solid state camera for detection is offered in invention according to claim 1.

[0011] In invention according to claim 2, it combines with the purpose of claim 1 and aims at the thing which enabled the output of the signal and picture signal of motion detection at coincidence and for which it moves and the solid state camera for detection is offered. In invention according to claim 3, it combines with the purpose of claim 2 and aims at offering the solid state camera for motion

detection which outputs the picture signal of the high quality which removed a part for a dark signal.

[0012] In invention according to claim 4, it combines with the purpose of claim 1 and aims at offering the solid state camera for motion detection which has the function to judge a motion of a photographic subject.

[0013]

[Means for Solving the Problem] Two or more light sensing portions which invention according to claim 1 is arranged in the shape of a matrix, and generate a signal charge according to incident light, (Claim 1) The amplifier which is prepared for every light sensing portion, has the regulatory region which accumulates a charge, and outputs the electrical signal corresponding to the stored charge of this regulatory region, The reset circuit which resets the regulatory region of an amplifier, and the charge transfer circuit which transmits the signal charge generated by the light sensing portion to the regulatory region of an amplifier, The perpendicular read-out line formed for every vertical file of a light sensing portion, and the readout circuitry which reads the electrical signal which is established for every amplifier and outputted from an amplifier to a perpendicular read-out line, In the condition [intercepting the transfer operation

of a charge transfer circuit and having made the signal charge of a front frame hold to regulatory region freely] Drive the readout circuitry of a specific line alternatively, drive the front frame perpendicular transfer means which reads the electrical signal of a front frame to a perpendicular read-out line, and the charge transfer circuit of a specific line, and the signal charge of the present frame is made to hold to regulatory region. In this condition The present frame perpendicular transfer means which drives the readout circuitry of a specific line and reads the electrical signal of the present frame to a perpendicular read-out line, The comparator circuit which compares the electrical signal of a front frame and the electrical signal of the present frame which are established for every perpendicular read-out line, and are read to time sharing through a perpendicular read-out line, The level transfer circuit which carries out the level transfer of each output from a comparator circuit, and the unnecessary charge discharge circuit which discharges the unnecessary charge which is prepared for every light sensing portion and generated by the light sensing portion, During the cutoff period of a charge transfer circuit, the unnecessary charge generated by the light sensing portion is discharged through an unnecessary charge discharge circuit, it has the electronic shutter circuit which restricts the storage time of the

signal charge in a light sensing portion, and the solid state camera for motion detection is constituted.

[0014] By such configuration, the signal charge of a front frame is held in the regulatory region of each amplifier with the solid state camera for motion detection according to claim 1. A front frame perpendicular transfer means outputs the electrical signal of the front frame outputted from an amplifier at this time to a perpendicular read-out line. On the other hand, after the signal charge of the present frame transmits the present frame perpendicular transfer means to the regulatory region of an amplifier, it outputs the electrical signal of the present frame outputted from an amplifier to a perpendicular read-out line.

[0015] "The electrical signal of a front frame" and "the electrical signal of the present frame" are outputted to a perpendicular read-out line by such actuation at time sharing. In a comparator circuit, "the electrical signal of a front frame" and "the electrical signal of the present frame" by which a time-sharing output is carried out in this way are incorporated for every perpendicular read-out line, and these comparisons are performed. In a level transfer circuit, the level transfer of the output of a comparator circuit is carried out, and it outputs as a motion detecting signal.

[0016] Moreover, the unnecessary charge discharge circuit which discharges the unnecessary charge of a light sensing portion in the solid state camera for motion detection according to claim 1, and the electronic shutter circuit which controls the unnecessary charge discharge circuit and realizes electronic shutter actuation are prepared especially. This electronic shutter circuit discharges the unnecessary charge of a light sensing portion through an unnecessary charge discharge circuit during cutoff of the transfer operation of a charge transfer circuit. Therefore, on the occasion of electronic shutter actuation, the signal charge of the front frame held at regulatory region is not spoiled.

[0017] In addition, although the expression a "frame" is used in the publication of claim 1, this is the original semantics of the image for one coma. The solid state camera for motion detection according to claim 1 does not need to be limited to what performs the Progres SHIBBU scan, for example, seems so, to perform interlace scanning. In such interlace scanning, based on a difference with the former front field, it moves from the present field and the present field, and detection is performed.

[0018] (Claim 2) In the solid state camera for motion detection according to claim 1, invention according to claim 2 incorporates alternatively either the electrical

signal of the front frame read to time sharing through a perpendicular read-out line, or the electrical signal of the present frame, and is characterized by having the picture signal output circuit which carries out a level transfer.

[0019] With such a configuration, since the electrical signal on a perpendicular read-out line is outputted alternatively, especially actuation of motion detection is not barred. Therefore, it becomes possible to output the signal and picture signal of motion detection to coincidence. Invention according to claim 3 is in the condition that the regulatory region of an amplifier was initialized by the fixed electrical potential difference by the drive of a reset circuit in the solid state camera for motion detection according to claim 2. (Claim 3) The dark signal perpendicular transfer means which reads the electrical signal (dark signal) which drives the readout circuitry of a specific line alternatively and is outputted from an amplifier to a perpendicular read-out line, It has the sample circuit which carries out the sample of the dark signal read to time sharing through a perpendicular read-out line, and a picture signal output circuit is characterized by outputting the signal which subtracted the part of the dark signal by which the sample was carried out to the sample circuit from either the "electrical signal of a front frame", or the "electrical signal of the present frame."

[0020] By such configuration, with the solid state camera for motion detection according to claim 3, a perpendicular read-out line is used efficiently and, in addition to the electrical signal for two frames, it outputs to time sharing to a dark signal. A picture signal output circuit becomes possible [outputting the quality electrical signal which removed the dark signal] by reducing the part of this dark signal from the electrical signal of a front frame or the present frame.

[0021] (Claim 4) It is characterized by the comparator circuit mentioned above in the solid state camera for motion detection given in any 1 term of claim 1 thru/or claim 3 being a circuit which judges whether the electrical signal of the present frame and the electrical signal of a front frame are in tolerance, and it is in agreement, and outputs a binary-ized signal according to the truth of a judgment result.

[0022] "The motion detecting signal made binary" which shows directly whether there was any change between a front frame and the present frame from the solid state camera for motion detection according to claim 4 by such configuration is outputted.

[0023]

[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention

is explained based on a drawing.

[0024] (1st operation gestalt) The 1st operation gestalt is an operation gestalt corresponding to invention according to claim 1 to 3. Drawing 1 is drawing showing the circuitry of the 1st operation gestalt. In drawing 1 , the matrix array of the unit pixel 11 is carried out at the solid state camera 10 for motion detection at a n line m train. Common connection of the output of these unit pixels 11 is made for every vertical file, and it forms the perpendicular read-out line 12 of m duty.

[0025] Moreover, the perpendicular transfer circuit 15 for determining the timing of a perpendicular transfer as the solid state camera 10 for motion detection is arranged. From this perpendicular transfer circuit 15, four kinds of control pulse phiTG1, phiRSG1, phiVA1, and phiRSP1 are supplied to the unit pixel 11 of the 1st line, respectively. Similarly, four kinds of control pulse phiTG2-n outputted from the perpendicular transfer circuit 15, phiRSG2-n, phiVA2-n, and phiRSP2-n are supplied also to the remaining unit pixels 11 of the 2-n-th line, respectively.

[0026] the current source 20 for supplying a bias current to the perpendicular read-out line 12 of the above-mentioned m duty, and difference -- processing circuit 21a (double sampling circuit) and dynamic body detector 21b (double

sampling circuit) are connected, respectively. these m difference -- control pulse phiN is supplied to the sample control terminal of processing circuit 21a in common. Such control pulse phiN is outputted from the perpendicular transfer circuit 15 etc. moreover, m difference -- common connection of all the outputs of processing circuit 21a is made, and they form level read-out line 16a for picture signals. The picture signal outputted on this level read-out line 16a is outputted to the exterior of the solid state camera 10 for motion detection through an internal video amplifier circuit etc.

[0027] On the other hand, control pulse phiM is supplied to m sample control terminals of dynamic body detector 21b in common. Such control pulse phiM is outputted from the perpendicular transfer circuit 15 etc. Moreover, common connection of all of the output of dynamic body detector 21b of m pieces is made, and it forms level read-out line 16b for motion detecting signals. The motion detecting signal outputted on this level read-out line 16b is outputted to the exterior of the solid state camera 10 for motion detection through an internal video amplifier circuit etc.

[0028] Moreover, the level transfer circuit 18 for determining the timing of a level transfer as the solid state camera 10 for motion detection is arranged. the

difference of eye 1 from this level transfer circuit 18 train -- a control pulse phiH1 is supplied in common to the level control terminal of processing circuit 21a and dynamic body detector 21b. the same -- carrying out -- the remaining difference of eye 2 - m train -- the control pulse phiH2 outputted from the level transfer circuit 18 - phiHm are supplied to the level control terminal of processing circuit 21a and dynamic body detector 21b, respectively.

[0029] Moreover, the MOS switches 19a and 19b for reset are connected to the level read-out lines 16a and 16b, respectively. Control pulse phiRH for reset is supplied to the gate of these MOS switches 19a and 19b. Such a control pulse phiRH is outputted from the level transfer circuit 18 etc. In addition, although not shown in drawing 1 , the MOS switch for reset etc. may be formed also like the perpendicular read-out line 12.

[0030] (Circuitry of the unit pixel 11) Next, based on drawing 1 , connection relation is explained to concrete circuitry and a list about the unit pixel 11 located in eye an one-line train [one train]. In addition, also about the other unit pixels 11, the suffixes of a control pulse only differ and the unit pixel 11 and circuitry of eye an one-line train [one train] are the same.

[0031] First, the photo diode 1 of an embedding mold is arranged at this unit

pixel 11. The anode of this photo diode 1 is connected to the gate of JFET (junction type FET)2 through the MOS switch 3 for a charge transfer. Control pulse phiTG1 outputted from the perpendicular transfer circuit 15 is supplied to the gate of the MOS switch 3 for this charge transfer.

[0032] Moreover, the gate of JFET2 is connected to metal wiring 7a maintained at fixed reset potential through the MOS switch 4 for signal-charge reset. Control pulse phiRSG1 outputted from the perpendicular transfer circuit 15 is supplied to the gate of this MOS switch 4. Furthermore, between the anode of photo diode 1 and metal wiring 7a is bypassed, and the MOS switch 5 for charge discharge is arranged. Control pulse phiRSP1 outputted from the perpendicular transfer circuit 15 is supplied to the gate of this MOS switch 5.

[0033] Moreover, the source of JFET2 is connected to the perpendicular read-out line 12 through the MOS switch 6 for a perpendicular transfer. Control pulse phiVA1 outputted from the perpendicular transfer circuit 15 is supplied to the gate of this MOS switch 6.

[0034] (Difference circuitry of processing circuit 21a and dynamic body detector 21b) next, the difference prepared in eye 1 of the perpendicular read-out line 12 train based on drawing 1 -- concrete circuitry is explained about processing

circuit 21a. in addition, the difference of 2 train henceforth -- a part of suffixes of a control pulse only differ also about processing circuit 21a -- it is -- the difference of eye one train -- processing circuit 21a and circuitry are the same.

[0035] First, the end of capacitor 22a for holding a dark signal is connected to the perpendicular read-out line 12. MOS switch 23a for giving fixed potentials, such as touch-down potential, and MOS switch 24a for a level transfer are connected to the other end of this capacitor 22a. The opposite side of this MOS switch 24a is connected to level read-out line 16a. Here, control pulse phiN is supplied to MOS switch 23a. Moreover, the control pulse phiH1 outputted from the level transfer circuit 18 is connected to MOS switch 24a.

[0036] Next, concrete circuitry is explained about dynamic body detector 21b prepared in eye 1 of the perpendicular read-out line 12 train. In addition, also about dynamic body detector 21b of 2 train henceforth, a part of suffixes of a control pulse only differ, and dynamic body detector 21b of eye one train and circuitry are the same. First, the end of capacitor 22b for holding the electrical signal of a front frame is connected to the perpendicular read-out line 12. MOS switch 23b for giving fixed potentials, such as touch-down potential, and MOS switch 24b for a level transfer are connected to the other end of this capacitor

22b. The opposite side of this MOS switch 24b is connected to level read-out line 16b. Here, control pulse phiM is supplied to MOS switch 23b. Moreover, the control pulse phiH1 outputted from the level transfer circuit 18 is connected to MOS switch 24b.

[0037] (Semi-conductor structure of the unit pixel 11) Next, the semi-conductor structure of the unit pixel 11 is explained using drawing 2 and drawing 3 . First, the unit pixel 11 is formed all over n mold field 31 formed in the principal plane side of a substrate 30 so that it may be shown in drawing 3 . p mold are recording field 35 is shape[of a field]-formed in the center of this n mold field 31 near the front face. n mold field for preventing depletion-ization of an oxide-film interface is thinly established in the top face of this p mold are recording field 35. The photo diode 1 of an embedding mold is constituted by the pn junction made to the perimeter of such a p mold are recording field 35.

[0038] Gate field 2G of JFET2 are allotted to one place of this p mold are recording field 35 perimeter through the gate field of the MOS switch 3 for a charge transfer. The path of n mold field which connects source 2S and drain 2D of JFET2 is established in this interior of gate field 2G. Wiring layers, such as polish recon to which control pulse phiTG1 was impressed, pass through an

oxide film in right above the gate field of the MOS switch 3 (see drawing 3 (b)).

[0039] Here, the drain 2D side of JFET2 contacts n mold field 31 soon, and is maintained at constant potential. On the other hand, the source 2S side is connected to one main electrode (here p mold field) of the MOS switch 6 for a perpendicular transfer through wiring 32. Wiring layers, such as polish recon to which control pulse phiVA1 was impressed, pass through an oxide film in right above the gate field of this MOS switch 6 (see drawing 3 (a)). Moreover, the main electrode (here p mold field) of another side of the MOS switch 6 is connected to wiring which forms the perpendicular read-out line 12.

[0040] On the other hand, the drain section 7 for discharge through the gate field of the MOS switch 4 is formed so that gate field 2G of JFET2 may be adjoined. Wiring layers, such as polish recon to which control pulse phiRSG1 was impressed, pass through an oxide film in right above the gate field of this MOS switch 4 (see drawing 3 (a)). Moreover, the gate field of the MOS switch 5 is prepared between the drain section 7 for discharge, and p mold are recording field 35. Right above the gate field of this MOS switch 5, wiring layers, such as polish recon to which control pulse phiRSP1 was impressed, pass (see drawing 3 (c)).

[0041] Thus, the drain section 7 for discharge constitutes the common drain of the MOS switch 4 and the MOS switch 5. This drain section 7 for discharge is maintained at fixed reset potential through metal wiring 7a. In addition, as shown in drawing 3 , in order that this metal wiring 7a may serve as a light-shielding film, the field except the light sensing portion of photo diode 1 is formed in a wrap configuration (in addition by drawing 2 , illustration of metal wiring 7a is omitted).

[0042] Here (Correspondence relation between this invention and the 1st operation gestalt) About the correspondence relation between invention according to claim 1 and the 1st operation gestalt A light sensing portion corresponds to photo diode 1, and an amplifier corresponds to JFET2. The regulatory region of an amplifier corresponds to gate field 2G, and a reset circuit corresponds to the MOS switch 4. A charge transfer circuit corresponds to the MOS switch 3, and a perpendicular read-out line is equivalent to the perpendicular read-out line 12. A readout circuitry corresponds to the MOS switch 6, and a front frame perpendicular transfer means corresponds to "the function which carries out the perpendicular transfer of the electrical signal of a front frame" of the perpendicular transfer circuit 15. The present frame perpendicular transfer means corresponds to "the function which carries out the

perpendicular transfer of the electrical signal of the present frame" of the perpendicular transfer circuit 15. A comparator circuit corresponds to dynamic body detector 21b, and a level transfer circuit corresponds to "the function which carries out the level transfer of the motion detecting signal" of the level transfer circuit 18. An unnecessary charge discharge circuit corresponds to the MOS switch 5, and an electronic shutter circuit corresponds to "the function to drive the MOS switch 5 and to restrict the storage time of photo diode 1" of the perpendicular transfer circuit 15.

[0043] moreover -- the correspondence relation between invention according to claim 2 and the 1st operation gestalt -- above-mentioned correspondence relation -- in addition, a picture signal output circuit -- difference -- it corresponds to "the function which carries out the level transfer of the picture signal of the present frame alternatively" of processing circuit 21a and the level transfer circuit 18. furthermore -- the correspondence relation between invention according to claim 3 and the 1st operation gestalt -- above-mentioned correspondence relation -- in addition, a dark signal perpendicular transfer means -- "the function which carries out the perpendicular transfer of the dark signal component of JFET2" of the perpendicular transfer circuit 15 -- corresponding -- a sample

circuit -- difference -- it corresponds to "the function which carries out the sample of the dark signal" of processing circuit 21a.

[0044] (Actuation of the 1st operation gestalt) Drawing 4 is a timing chart which shows the drive timing of the 1st operation gestalt. In addition, this Fig. shows pixel train read-out after the horizontal of the i-th line. Hereafter, actuation of the 1st operation gestalt is explained using drawing 4 . First, in the timing of the period T1 shown in drawing 4 , control pulse phiRSPi is brought down to a low level. Then, in the unit pixel 11 of the horizontal of the i-th line, the MOS switch 5 flows and the unnecessary charge accumulated in photo diode 1 at the time is discharged. Just before [termination] this period T1, since control pulse phiRSPi returns high-level, the unit pixel 11 of the horizontal of the i-th line resumes are recording of a signal charge from just before [termination] this period T1.

[0045] Next, in initiation of the perpendicular transfer operation of eye a level i line, in the timing of the period T2 shown in drawing 4 , control pulse phiVAi is held to a low level, and control pulse phiM is started high-level. this control pulse phiVAi -- bringing down -- the MOS switch 6 of the horizontal of the i-th line flows. At this time, the signal charge accumulated on the occasion of read-out of a front

frame remains in gate field 2G of JFET2. Therefore, a front frame and the electrical signal of the horizontal of the i-th line are outputted on the perpendicular read-out line 12 through the source follower circuit of JFET2. On the other hand, in the dynamic body detector 21b side, MOS switch 23b flows by starting of control pulse phiM. Consequently, the charge path which passes along capacitor 22b is formed, and a front frame and the electrical signal of the horizontal of the i-th line are charged by capacitor 22b in dynamic body detector 21b. Since control pulse phiM is brought down just before [termination] this period T2, the end of capacitor 22b will be in floating again. Consequently, a front frame and the electrical signal of the horizontal of the i-th line are held as a both-ends electrical potential difference of a capacitor 22b group.

[0046] Next, in the timing of period T3 shown in drawing 4 , control pulse phiRSGi is brought down to a low level. Then, in the unit pixel 11 of the horizontal of the i-th line, the MOS switch 4 flows and the signal charge of the front frame which remained to gate field 2G of JFET2 is discharged. Consequently, gate field 2G are initialized by the reset electrical potential difference through metal wiring 7a. Since a control pulse VAi is still maintained by the low level at this time, dispersion in the electrical potential difference

between the gate-sources produced in JFET2 of the horizontal of the i-th line (dark signal) is outputted to the perpendicular read-out line 12.

[0047] Then, in the timing of period T four shown in drawing 4 , control pulse phiN is started high-level. difference -- in the processing circuit 21a side, MOS switch 23a flows by starting of control pulse phiN. consequently, the charge path which passes along capacitor 22a forms -- having -- the dark signal of the horizontal of the i-th line -- difference -- capacitor 22a in processing circuit 21a charges. Since control pulse phiN is brought down just before [termination] this period T four, the end of capacitor 22a will be in floating again. Consequently, the dark signal of the horizontal of the i-th line is held as a both-ends electrical potential difference of a capacitor 22a group.

[0048] Next, control pulse phiTGi is brought down by the low level in the timing of the period T5 shown in drawing 4 . Then, in the unit pixel 11 of the horizontal of the i-th line, the MOS switch 3 flows and the signal charge of the present frame accumulated in the photo diode 1 of the horizontal of the i-th line is transmitted to gate field 2G of JFET2. In addition, the storage time (exposure time) of a signal charge here corresponds to the period Tex of just before [termination] a period T1 to the initiation time of a period T5.

[0049] In this condition, since control pulse phiVAi is still a low level, from the perpendicular read-out line 12, the present frame and the electrical signal of the horizontal of the i-th line are newly outputted. Therefore, in the end side of capacitor 22b by the side of dynamic body detector 21b, the difference which reduced the front frame and the electrical signal of the horizontal of the i-th line appears from the electrical signal of the present frame and the horizontal of the i-th line. Since this difference expresses an inter-frame difference, it serves as a motion detecting signal.

[0050] on the other hand -- difference -- in the end side of capacitor 22a by the side of processing circuit 21a, the difference which reduced a part for the dark signal of the horizontal of the i-th line appears from the electrical signal of the present frame and the horizontal of the i-th line. This difference is "the picture signal of the present frame" with which the dark signal component was removed.

[0051] Next, it sets to the timing of the period T6 shown in drawing 4 , and the level transfer circuit 18 is a control pulse phiH1... Turns is taken and a sequential setup of the phiHm is carried out high-level. Therefore, the end side of capacitor 22b for m train is connected to level read-out line 16b in order of 1 - m train. consequently -- a level read-out line 16b top -- inter-frame [of the horizontal of

the i-th line] -- the motion detecting signal which shows difference is outputted one by one.

[0052] On the other hand, the end side of capacitor 22a for m train is connected to level read-out line 16a in order of 1 - m train. Consequently, on level read-out line 16a, the present frame and the picture signal of the horizontal of the i-th line are outputted one by one. In addition, it sets during a period T6 and is a control pulse phiH1... phiRH is set as the interval which sets up phiHm high-level high-level. The residual charge on level read-out line 16a and 16b is discharged through the MOS switches 19a and 19b by such actuation each time. Therefore, residual charge does not mix with the motion detecting signal and picture signal by which a level transfer is carried out. (Since a signal is outputted intermittently in this way, 0th hold actuation may be performed in the video amplifier circuit connected to the read-out lines 16a and 16b depending on the case.)

From level read-out line 16b, the motion detecting signal equivalent to one frame is outputted outside by repeating in order a series of processings mentioned above also about other water parallel. Moreover, from level read-out line 16a, the picture signal of the present frame is outputted outside.

[0053] In addition, supplementary information is performed about the exposure

period Tex. First, at the time of termination of the period T6 just before reading the pixel of the horizontal of the i+1st line, control pulse phiRSPi+r falls to a low level, and the unnecessary charge accumulated in the photo diode 1 of the pixel of eye a level i+r line is discharged. The photo diode 1 of the pixel of eye these level i+r line accumulates the period from this discharge point in time to read-out initiation of eye a level i+r line, and a signal charge. Therefore, the exposure time Tex of the 1st operation gestalt is mostly equivalent to the read-out time amount for a horizontal (r-1) line. Control pulse phiRSP1-n is outputted from the perpendicular transfer circuit 15 so that this exposure time Tex may become fixed about all pixels.

[0054] By actuation explained above, dynamic body detector 21b can generate a motion detecting signal with the 1st operation gestalt by taking the difference of the electrical signal for two frames by which a time-sharing output is carried out on the perpendicular read-out line 12. Therefore, in order to perform motion detection, the need of establishing circumference circuits, such as an AD translation circuit, and an image memory, an image-processing circuit, in the exterior of a solid state camera is absolutely none. Consequently, it becomes possible to constitute equipment at large [, such as supervisory equipment which

needs motion detection, and picture compression equipment,] in small and low cost.

[0055] Moreover, it moves by the 1st operation gestalt, without minding an AD translation circuit, and the detecting signal is generated. Therefore, a dynamic range is not restricted by the AD translation circuit and motion detection can be performed, using the large dynamic range of the solid state camera itself as it is. Furthermore, with the 1st operation gestalt, the configuration of a pixel can be simplified compared with the case where a comparator circuit is prepared for every pixel. Therefore, improvement in a numerical aperture and improvement in resolution can be aimed at comparatively easily.

[0056] Moreover, the electrical signal of a front frame and the electrical signal of the present frame are compared by the 1st operation gestalt without phase gap of a pixel location in a solid state camera. Therefore, the fault which incorrect-detects the edge part of an image with a motion in an external circuit compared with the case where an inter-frame difference is taken is lost entirely. Moreover, with the 1st operation gestalt, the unnecessary charge in photo diode 1 is soon discharged through the MOS switch 5 for charge discharge during the cutoff period of the MOS switch 3 for a charge transfer. According to such a

device, electronic shutter ability can be realized certainly, without giving trouble entirely to actuation of motion detection.

[0057] In the case where an image flows by early motion of a photographic subject especially, it becomes difficult to detect the location of a dynamic body to a precision based on an inter-frame difference. In such a case, it becomes possible by preventing the flow of an image using the above-mentioned electronic shutter actuation to realize precise motion detection.

[0058] Moreover, with the 1st operation gestalt, a picture signal can be outputted by outputting alternatively "the electrical signal of the present frame" by which a time-sharing output is carried out in the perpendicular read-out line 12 top. Especially output actuation such of a picture signal does not bar any motion detection actuation by the side of dynamic body detector 21b. Therefore, it becomes possible to output a motion detecting signal and a picture signal to coincidence. The dual output of these two kinds of signals becomes what was very suitable for the application which needs to detect a motion like supervisory equipment, observing an image (record).

[0059] Furthermore, with the 1st operation gestalt, the perpendicular read-out line 12 is used efficiently, and, in addition to the electrical signal for two frames, it

outputs to time sharing to a dark signal. difference -- in processing circuit 21a, the quality electrical signal which removed the dark signal can be acquired based on this dark signal. Next, another operation gestalt is explained.

[0060] (2nd operation gestalt) The 2nd operation gestalt is an operation gestalt corresponding to invention according to claim 1 to 4. Drawing 5 is drawing showing the circuitry of the 2nd operation gestalt. In drawing 5 , the matrix array of the unit pixel 11 is carried out at the solid state camera 40 for motion detection at a n line m train. Common connection of the output of these unit pixels 11 is made for every vertical file, and it forms the perpendicular read-out line 12 of m duty.

[0061] Moreover, the perpendicular transfer circuit 15 for determining the timing of a perpendicular transfer as the solid state camera 40 for motion detection is arranged. From this perpendicular transfer circuit 15, four kinds of control pulse phiTG1, phiRSG1, phiVA1, and phiRSP1 are supplied to the unit pixel 11 of the 1st line, respectively. Similarly, four kinds of control pulse phiTG2-n outputted from the perpendicular transfer circuit 15, phiRSG2-n, phiVA2-n, and phiRSP2-n are supplied also to the remaining unit pixels 11 of the 2-n-th line, respectively.

[0062] the current source 20 for supplying a bias current to the perpendicular

read-out line 12 of the above-mentioned m duty, and difference -- processing circuit 21a, different value detector 41b (after-mentioned), and MOS switch 20a for reset are connected, respectively. these m difference -- control pulse phiN is supplied to the sample control terminal of processing circuit 21a in common. Such control pulse phiN is outputted from the perpendicular transfer circuit 15 etc. moreover, m difference -- common connection of all the output terminals of processing circuit 21a is made, and they form level read-out line 16a for picture signals. The picture signal outputted on this level read-out line 16a is outputted to the exterior of the solid state camera 40 for motion detection through an internal video amplifier circuit etc.

[0063] Furthermore, MOS switch 19a for reset is connected to level read-out line 16a. Control pulse phiRH for reset is supplied to the gate of such MOS switch 19a. Such a control pulse phiRH is outputted from the level transfer circuit 18 etc. Moreover, the level transfer circuit 18 for determining the timing of a level transfer as the solid state camera 40 for motion detection is arranged. the difference of eye 1 from this level transfer circuit 18 train -- a control pulse phiH1 is supplied to the level control terminal of processing circuit 21a. the same -- carrying out -- the remaining difference of eye 2 - m train -- the control pulse

phiH2 outputted also to the level control terminal of processing circuit 21a from the level transfer circuit 18 - phiHm are supplied, respectively.

[0064] On the other hand, control pulse phiSA and phiSB are supplied to m sample control terminals of different value detector 41b. Such a control pulse phiSA and phiSB are outputted from the perpendicular transfer circuit 15 etc. Moreover, m output terminals Q of different value detector 41b are connected to the parallel input of a shift register 48, respectively. Control pulse phiLD and transfer clock phiCK for determining the incorporation timing of parallel data are inputted into this shift register 48. Such pulse phiLD and phiCK are supplied from the level transfer circuit 18 etc. Moreover, the serial output of a shift register 48 moves as a motion detecting signal, and is outputted to the exterior of the solid state camera 40 for detection.

[0065] in addition, the unit pixel 11 and difference -- about the internal configuration of processing circuit 21a, since it is the same as the 1st operation gestalt, the same reference number is given and it is shown in drawing 5 , and explanation here is omitted.

(Circuitry of different value detector 41b) Next, based on drawing 6 (a), concrete circuitry is explained about different value detector 41b prepared in eye 1 of the

perpendicular read-out line 12 train. In addition, also about different value detector 41b of 2 train henceforth, a part of suffixes of a control pulse only differ, and different value detector 41b of eye one train and circuitry are the same.

[0066] First, the end side of the MOS switches 42a and 42b is connected to the perpendicular read-out line 12 of eye one train, respectively. The other end side of this MOS switch 42a is connected to capacitor 43a for electrical-potential-difference maintenance, the forward side input of comparator 44a, and the negative side input of comparator 44b, respectively.

[0067] On the other hand, the other end side of MOS switch 42b is connected to capacitor 43b for electrical-potential-difference maintenance, the negative side input of comparator 44a, and the forward side input of comparator 44b, respectively. In addition, the input-output behavioral characteristics of these comparators 44a and 44b are shown in drawing 6 (b). Each output of these comparators 44a and 44b is inputted into OR circuit 45, respectively. The output of this OR circuit 45 is supplied to the parallel input Q1 of a shift register 48.

[0068] (Correspondence relation between this invention and the 2nd operation gestalt) Here about the correspondence relation between invention given in claims 1 and 4, and the 2nd operation gestalt A light sensing portion

corresponds to photo diode 1, and an amplifier corresponds to JFET2. The regulatory region of an amplifier corresponds to gate field 2G, and a reset circuit corresponds to the MOS switch 4. A charge transfer circuit corresponds to the MOS switch 3, and a perpendicular read-out line is equivalent to the perpendicular read-out line 12. A readout circuitry corresponds to the MOS switch 6, and a front frame perpendicular transfer means corresponds to "the function which carries out the perpendicular transfer of the electrical signal of a front frame" of the perpendicular transfer circuit 15. The present frame perpendicular transfer means corresponds to "the function which carries out the perpendicular transfer of the electrical signal of the present frame" of the perpendicular transfer circuit 15. A comparator circuit corresponds to different value detector 41b, and a level transfer circuit corresponds to a shift register 48. An unnecessary charge discharge circuit corresponds to the MOS switch 5, and an electronic shutter circuit corresponds to "the function to drive the MOS switch 5 and to restrict the storage time of photo diode 1" of the perpendicular transfer circuit 15.

[0069] moreover -- the correspondence relation between invention according to claim 2 and the 2nd operation gestalt -- above-mentioned correspondence

relation -- in addition, a picture signal output circuit -- difference -- it corresponds to "the function which carries out the level transfer of the picture signal of the present frame alternatively" of processing circuit 21a and the level transfer circuit 18. furthermore -- the correspondence relation between invention according to claim 3 and the 2nd operation gestalt -- above-mentioned correspondence relation -- in addition, a dark signal perpendicular transfer means -- "the function which carries out the perpendicular transfer of the dark signal component of JFET2" of the perpendicular transfer circuit 15 -- corresponding -- a sample circuit -- difference -- it corresponds to "the function which carries out the sample of the dark signal" of processing circuit 21a.

[0070] (Actuation of the 2nd operation gestalt) Drawing 7 is a timing chart which shows the drive timing of the 2nd operation gestalt. In addition, this Fig. shows pixel train read-out after the horizontal of the i-th line. Hereafter, actuation of the 2nd operation gestalt is explained using drawing 7 . First, in the timing of the period T1 shown in drawing 7 , control pulse phiRSPi is brought down to a low level. Then, in the unit pixel 11 of the horizontal of the i-th line, the MOS switch 5 flows and the unnecessary charge accumulated in photo diode 1 at the time is discharged. Just before [termination] this period T1, since control pulse

phiRSPi returns high-level, the unit pixel 11 of the horizontal of the i-th line resumes are recording of a signal charge from just before [termination] this period T1.

[0071] Next, in initiation of the perpendicular transfer operation of eye a level i line, in the timing of the period T2 shown in drawing 7 , control pulse phiVAi is held to a low level, and control pulse phiM is started high-level. this control pulse phiVAi -- bringing down -- the MOS switch 6 of the horizontal of the i-th line flows. At this time, the signal charge accumulated on the occasion of read-out of a front frame remains in gate field 2G of JFET2. Therefore, a front frame and the electrical signal of the horizontal of the i-th line are outputted to the perpendicular read-out line 12 through the source follower circuit of JFET2. On the other hand, at the different value detector 41b side, control pulse phiSA is started to the timing of this period T2. Therefore, MOS switch 42a flows and the charge path which passes along the perpendicular read-out line 12 and capacitor 43a is formed. Consequently, a front frame and the electrical signal of the horizontal of the i-th line are charged by capacitor 43a in different value detector 41b. Since control pulse phiSA is brought down just before [termination] this period T2, the end of capacitor 43a is again separated from

the perpendicular read-out line 12. Consequently, a front frame and the electrical signal of the horizontal of the i-th line are held as a both-ends electrical potential difference of capacitor 43a.

[0072] Next, in the timing of period T3 shown in drawing 7 , control pulse phiRSGi is brought down to a low level. Then, in the unit pixel 11 of the horizontal of the i-th line, the MOS switch 4 flows and the signal charge of the front frame which remained to gate field 2G of JFET2 is discharged. Consequently, gate field 2G are initialized by the reset electrical potential difference through metal wiring 7a. Since a control pulse VAi is still maintained by the low level at this time, dispersion in the electrical potential difference between the gate-sources produced in JFET2 of the horizontal of the i-th line (dark signal) is outputted to the perpendicular read-out line 12.

[0073] Then, in the timing of period T four shown in drawing 7 , control pulse phiN is started high-level. difference -- in the processing circuit 21a side, MOS switch 23a flows by starting of control pulse phiN. consequently, the charge path which passes along the perpendicular read-out line 12 and capacitor 22a forms -- having -- the dark signal of the horizontal of the i-th line -- difference -- capacitor 22a in processing circuit 21a charges. Since control pulse phiN is

brought down just before [termination] this period T four, the end of capacitor 22a will be in floating again. Consequently, the dark signal of the horizontal of the i-th line is held as a both-ends electrical potential difference of capacitor 22a.

[0074] Next, control pulse phiTGi is brought down by the low level in the timing of the period T5 shown in drawing 7 . Then, in the unit pixel 11 of the horizontal of the i-th line, the MOS switch 3 flows and the signal charge of the present frame accumulated in the photo diode 1 of the horizontal of the i-th line is transmitted to gate field 2G of JFET2. In addition, the storage time (exposure time) of a signal charge here corresponds to the period Tex of just before [termination] a period T1 to the initiation time of a period T5.

[0075] In this condition, since control pulse phiVAi is still a low level, from the perpendicular read-out line 12, the present frame and the electrical signal of the horizontal of the i-th line are newly outputted. this time -- difference -- in the end side of capacitor 22a by the side of processing circuit 21a, the difference which reduced a part for the dark signal of the horizontal of the i-th line appears from the electrical signal of the present frame and the horizontal of the i-th line. This difference is "the picture signal of the present frame" with which the dark signal component was removed.

[0076] Next, in the timing of the period T6 shown in drawing 7 , control pulse phiSB is started and MOS switch 42b in dynamic body detector 41b flows. Consequently, the charge path which passes along the perpendicular read-out line 12 and capacitor 43b is formed, and the present frame and the electrical signal of the horizontal of the i-th line are charged by capacitor 43b in different value detector 41b. Since control pulse phiSB is brought down just before [termination] this period T6, the end of capacitor 43b is again separated from the perpendicular read-out line 12. Consequently, a front frame and the electrical signal of the horizontal of the i-th line are held as a both-ends electrical potential difference of capacitor 43b.

[0077] Here, Comparators 44a and 44b have the input-output behavioral characteristics shown in drawing 6 (b). Therefore, if the absolute value of the electrical-potential-difference difference of Capacitors 43a and 43b exceeds threshold deltaV, it will become high-level one of outputting [of Comparators 44a and 44b], and the output of OR circuit 45 will become high-level. Moreover, if the absolute value of the electrical-potential-difference difference of Capacitors 43a and 43b is less than threshold deltaV, the output of the both sides of Comparators 44a and 44b will serve as a low level, and the output of OR circuit

45 will serve as a low level.

[0078] In just before [termination] this period T6, each above-mentioned output of OR circuit 45 is incorporated by the parallel input of a shift register 48 by starting control pulse phiLD of a shift register 48, respectively. Next, the level transfer circuit 18 is a control pulse phiH1 during the period T7 shown in drawing 7 ... Turns is taken and a sequential setup of the phiHm is carried out high-level.

[0079] Therefore, the end side of capacitor 22a for m train is connected to level read-out line 16a in order of 1 - m train. Consequently, on level read-out line 16a, the present frame and the picture signal of the horizontal of the i-th line are outputted one by one. It sets during this period T6, and is a control pulse phiH1... phiRH is set as the interval which sets up phiHm high-level high-level. The residual charge on level read-out line 16a is discharged through MOS switch 19a by such actuation each time. Therefore, residual charge does not mix with the picture signal by which a level transfer is carried out.

[0080] Moreover, transfer clock phiCK is given to a shift register 48 one by one during this period T7. Consequently, each judgment result of different value detector 41b incorporated in the shift register 48 is transmitted horizontally, and is outputted one by one as a motion detecting signal made binary. From a shift

register 48, the external output of the motion detecting signal equivalent to one frame is carried out by repeating in order a series of processings mentioned above also about other water parallel. Moreover, from level read-out line 16a, the external output of the picture signal of the present frame is carried out.

[0081] By actuation explained above, the same effectiveness as the 1st operation gestalt can be acquired with the 2nd operation gestalt. especially, as effectiveness peculiar to the 2nd operation gestalt, whether a front frame and the present frame are equal in tolerance (here threshold deltaV) judges for every pixel in different value detector 41b -- having -- the judgment result -- "-- it is the point which was made binary and by which moves and an external output is carried out as detecting-signal."

[0082] Thus, since the motion detecting signal is already made binary, it becomes possible to simplify a motion judging in the equipment exterior etc. Moreover, since the motion detecting signal is made binary, it becomes possible to use a shift register 48 for a level transfer circuit, and improvement in the speed and low noise-ization can be easily realized in the level transfer operation of a motion detecting signal. In addition, although JFET2 is used as an amplifier and the signal charge is accumulated in gate field 2G of JFET2 with the

operation gestalt mentioned above, it is not limited to especially this configuration. Generally, the component which has a magnification function can be used as an amplifier. For example, an MOS transistor, a bipolar transistor, etc. may be used as an amplifier, and the functional device which carried out mixture use of these components may be used. Moreover, a signal charge may be held to the parasitic capacitance generated at the gate and the base of these amplifiers, and the capacitor for holding a signal charge etc. may be formed in the gate and the base of an amplifier auxiliary.

[0083] Furthermore, with the operation gestalt mentioned above, as a readout circuitry, although the MOS switch 6 for a perpendicular transfer is formed, it is not limited to this. For example, connection and separation with an amplifier and a perpendicular read-out line may be controlled by forming the capacitor for accumulating a signal charge in the gate and the base of an amplifier, and making the electrical potential difference by the side of the other end of this capacitor go up and down.

[0084] Moreover, although the operation gestalt mentioned above explained the case where transfer direct of the signal charge produced with photo diode was carried out to the regulatory region of an amplifier, this invention is not limited to

this. For example, after transmitting a signal charge to a diffusion field and holding it, the potential of the diffusion field may be detected through a signal line at the gate of an MOS transistor. As an example of such a pixel, they are reference "Active Pixel Sensors:Are CCD's Dinosaurs?", Fossum E.R., and Proceeding of SPIE, for example. : There are Charge-Coupled Device and Solid StateOptical SensorsIII, Vol.1900, and a thing described at pp 2-14 (1993).

[0085] Furthermore, although the operation gestalt mentioned above explained the case where the unit pixel 11 was arranged in the shape of a two-dimensional matrix, of course, this invention can apply similarly to the Rhine image sensor arranged in the shape of a 1-dimensional matrix. In addition, especially with the 2nd operation gestalt mentioned above, although MOS switch 20a is not driven, it is not limited to this. For example, in the intervals of a signal transfer of time sharing on the perpendicular read-out line 12, control pulse phiVA1-n may once be set as a low level, and control pulse phiRSV may be momentarily started in this condition. Such actuation enables it to discharge the residual charge on the perpendicular read-out line 12 at a high speed through MOS switch 20a. Usually, for the capacitive load which is parasitic on the perpendicular read-out line 12, the source follower output of JFET2 does not function effectively in the case of

sag, but the electrical potential difference of the perpendicular read-out line 12 falls according to the drawing-in current of a constant current source 20 chiefly. The above-mentioned reset action of MOS switch 20a can make actuation of the sag of this perpendicular read-out line 12 complete promptly. Therefore, such a reset action of MOS switch 20a serves as an effective cure, when attaining much more improvement in the speed of perpendicular read-out actuation.

[0086] Moreover, although different value detector 41b as shown in drawing 6 is used with the 2nd operation gestalt mentioned above, it is not limited to this configuration. If it is the judgment circuit which generally judges whether the electrical signal is in agreement, it can be used as a different value detector. For example, different value detector 51b as shown in drawing 8 can also be used. Hereafter, actuation of this different value detector 51b is explained.

[0087] First, control pulse phiSC is temporarily started to the timing by which the pixel output Vold of a front frame is outputted to the perpendicular read-out line 12. Consequently, the MOS switches QB1 and QB2 flow, and the charge path through Capacitors CCA and CCB is formed.

[0088] At this time, the electrical potential difference of (Vold-VT+Vth) is held in the both ends of Capacitor CCA. On the other hand, in the both ends of

Capacitor CCB, the electrical potential difference of (Vold-VT-Vth) is held. Next, if the pixel output Vnow of the present frame is outputted to the perpendicular read-out line 12, in the other end side of Capacitor CCA, the electrical-potential-difference value of (Vnow-Vold+VT-Vth) will appear. On the other hand, in the other end side of Capacitor CCB, the electrical-potential-difference value of (Vnow-Vold+VT+Vth) appears. In addition, the threshold voltage of inverters INV1 and INV2 is set as VT.

[0089] With the above electrical-potential-difference relation, if (Vnow-Vold) exceeds VTh, an inverter INV1 will output a low level. On the other hand, if (Vnow-Vold) is less than VTh, an inverter INV1 will output high level. Moreover, if (Vnow-Vold) exceeds (-VTh), an inverter INV2 will output a low level. On the other hand, if (Vnow-Vold) is less than (-VTh), an inverter INV2 will output high level.

[0090] After such fanout minds inverters 3-INV 5, it is inputted into NAND circuit NA, respectively. Consequently, from NAND circuit NA, when the value of (Vnow-Vold) is within the limits of -(- VTh) VTh, a low level is outputted. Moreover, high level is outputted when there is a value of (Vnow-Vold) out of range [-(-VTh) VTh].

[0091] In addition, the MOS switches QB3 and QB4 flow by starting control pulse phiSD to the timing as which such fanout was determined. Consequently, through inverters INV3 and INV4, the recharge of the capacitors CCA and CCB is carried out in the direction of positive feedback, and they can stabilize fanout. By such circuit actuation, it can judge whether a 2 inter-frame pixel output is in tolerance, and it is in agreement using different value detector 51b. Therefore, it replaces with different value detector 41b shown in drawing 5 , and it becomes possible to prepare different value detector 51b.

[0092]

[Effect of the Invention] (Claim 1) As explained above, in invention of claim 1, "the electrical signal of a front frame" and "the electrical signal of the present frame" are outputted on a perpendicular read-out line at time sharing. By comparing these electrical signals, it can move in the interior of a solid state camera, and detection can be realized.

[0093] Therefore, it can move without establishing especially circumference circuits, such as an AD translation circuit, and an image memory, an image-processing circuit, in the exterior of a solid state camera, and can detect. Therefore, it becomes possible to constitute the whole equipment in small and

low cost. Moreover, in invention of claim 1, the AD translation circuit which was the need conventionally becomes unnecessary to the exterior of the solid state camera for motion detection. Consequently, it becomes without a dynamic range being restricted by the AD translation circuit, and the large dynamic range of the solid state camera itself can perform motion detection.

[0094] Furthermore, in invention of claim 1, the configuration of a pixel can be simplified compared with the case where a comparator circuit is prepared for every pixel. Therefore, improvement in a numerical aperture and improvement in resolution can be aimed at. Moreover, in a solid state camera, a pixel location does not shift and the electrical signal of a front frame and the electrical signal of the present frame are compared by invention of claim 1. Therefore, compared with the case where an inter-frame difference is taken in an external circuit, a possibility of producing incorrect detection of the motion by phase gap of a pixel location becomes possible [performing motion detection with high precision much more] absolutely none.

[0095] Moreover, by invention, the unnecessary charge of a light sensing portion is soon discharged through an unnecessary charge discharge circuit during the cutoff period of a charge transfer circuit to claim 1. Electronic shutter ability is

certainly realizable with such actuation.

[0096] Moreover, since actuation of such an electronic shutter is performed at the cutoff period of a charge transfer circuit, the signal charge of the front frame held to regulatory region is not spoiled. Therefore, electronic shutter ability can be realized, without giving trouble entirely to actuation of motion detection. When an image flows by early motion of a photographic subject especially, it becomes difficult to operate the motion detection based on an inter-frame difference to a precision. Therefore, this invention which has the electronic shutter ability which does not give trouble to actuation of motion detection as mentioned above is a configuration especially suitable as a solid state camera for motion detection.

[0097] (Claim 2) In invention according to claim 2, a picture signal can be outputted by outputting alternatively either "the electrical signal of a front frame" outputted to time sharing in a perpendicular read-out line top, or "the electrical signal of the present frame." Since such output actuation of a picture signal is performed without barring entirely the motion detection actuation by the side of a comparator circuit, it becomes possible [carrying out the dual output of the signal and picture signal of motion detection].

[0098] especially, it moves with such a picture signal, and by the dual output of a

detecting signal, the variation of the image display using both [these] signals is markedly alike, and increases, and the application of the solid state camera for motion detection spreads remarkably. (Claim 3) In invention according to claim 3, a perpendicular read-out line is used efficiently and, in addition to the electrical signal for two frames, it outputs to time sharing to a dark signal. In a sample circuit side, the quality electrical signal which removed the dark signal is generated based on this dark signal.

[0099] Since especially the perpendicular transfer operation of such a dark signal is made in the intervals of the perpendicular transfer operation of the electrical signal for two frames, it does not produce any trouble in actuation of motion detection. Therefore, it becomes possible to carry out the dual output of the signal of motion detection, and the quality picture signal.

[0100] (Claim 4) invention according to claim 4 shows per pixel whether there was any change between a front frame and the present frame by actuation of a comparator circuit -- it was made binary -- it moves and a detecting signal is outputted. It moves and such a thing that was made binary and that simplify a motion judging in the equipment exterior etc. becomes possible by the detecting signal. Moreover, since the motion detecting signal is made binary, a shift

register circuit can be used for a level transfer circuit. In the level transfer operation of a motion detecting signal, improvement in the speed and low noise-ization are easily realizable with use of such a shift register circuit.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is drawing showing the circuitry of the 1st operation gestalt.

[Drawing 2] It is drawing explaining the sample layout of the unit pixel 11.

[Drawing 3] It is drawing explaining the cross-section structure of each part of the unit pixel 11.

[Drawing 4] It is the timing chart which shows the drive timing of the 1st operation gestalt.

[Drawing 5] It is drawing showing the circuitry of the 2nd operation gestalt.

[Drawing 6] It is drawing showing the circuitry of different value detector 41b.

[Drawing 7] It is the timing chart which shows the drive timing of the 2nd operation gestalt.

[Drawing 8] It is drawing showing the example of a circuit of a different value detector.

[Drawing 9] It is drawing showing the conventional image processing system 100 for motion detection.

[Description of Notations]

1 Photo Diode

2 JFET

2G Gate field

2S Source

2D Drain

3 MOS Switch for Charge Transfer

4 MOS Switch for Signal-Charge Reset

5 MOS Switch for Charge Discharge

6 MOS Switch for Perpendicular Transfer

7 Drain Section for Discharge

7a Metal wiring

10 Solid State Camera for Motion Detection

11 Unit Pixel

12 Perpendicular Read-out Line

15 Perpendicular Transfer Circuit

16a Level read-out line

16b Level read-out line

18 Level Transfer Circuit

19a, 19b MOS switch

21a difference -- a processing circuit

21b Dynamic body detector

22a Capacitor

23a MOS switch

24a The MOS switch for a level transfer

30 Substrate

31 N Mold Field

35 P Mold Are Recording Field

40 Solid State Camera for Motion Detection

41b Different value detector

42a MOS switch

43a Capacitor

44a Comparator

44b Comparator

45 OR Circuit

48 Shift Register

51b Different value detector